AMENDMENTS TO THE CLAIMS

Please amend Claims 24 and 27 as follows.

LISTING OF CLAIMS

1.-23. (canceled)

24. (currently amended) A power semiconductor device comprising:

a CZ (Czochralski) semiconductor substrate doped at an impurity concentration of between $7x10^{18} - 1x10^{21} cm^{-3}$, said semiconductor substrate having a roughened rear surface a surface concentration of which is given by said impurity concentration;

a semiconductor layer disposed over the semiconductor substrate;

a power semiconductor element formed at a surface portion of the semiconductor layer;

a first metal layer forming a first electrode of said power semiconductor element, the first metal layer being located over said surface portion; and

a second metal layer forming a second electrode of said power semiconductor element, the second metal layer being located to contact said roughened rear surface of said semiconductor substrate.

25. (previously presented) A power semiconductor device according to Claim 24, wherein said semiconductor substrate is doped with arsenic at an arsenic concentration of between $7x10^{18} - 1x10^{21} cm^{-3}$, said surface concentration of said roughened rear surface being given by said arsenic concentration.

26. (previously presented) A power semiconductor device according to Claim 24, wherein said second metal layer comprises a metal selected from a group consisting of titanium (Ti), vanadium (V), chromium (Cr) and nickel (Ni).

27. (currently amended) A power semiconductor device according to Claim 24, wherein a thickness [[form]] <u>from</u> a surface of said first metal layer to said roughened rear surface of said semiconductor substrate is 200 – 450 microns.

28. (previously presented) A power semiconductor device according to Claim 24, wherein said roughened rear surface of said semiconductor substrate has a surface roughness of between 0.2 – 0.6 microns.